PXIe/PCIe-5510/5511/5512

32 通道 18 位 高精度数据采集卡

PXIe-5510

特点

- 32 路单端模拟输入
- 模拟输入范围分为 7 档：
  ±10V/±5V/±2V/±1V/±0.5V/±0.2V/±0.1V
- 板载 64M 采样点模拟输入 FIFO
- DMA，用于模拟输入输出
- 4 通道 16 位同步模拟输出，
  带波形发生功能
- 板载 32M 采样点模拟输出 FIFO
- 32 通道 4 组 (4 个 Port)TTL 数字输入输出
- 4 通道 32 位通用定时器 / 计数器
- 模拟 / 数字触发

订购指南

- PXIe/PCIe-5510
  32 通道 18-bit, 2 MS/s 高精度数据采集卡
- PXIe/PCIe-5511
  32 通道 18-bit, 1.25 MS/s 高精度数据采集卡
- PXIe/PCIe-5512
  32 通道 18-bit, 500 kS/s 高精度数据采集卡

配件

Product Name	Description	PN
ACL-2006868-1	1M 68pin VHDCI68M-SCSI68M cable	JY2006868-01
DIN-68S-01	SCSI 68-pin Terminal board w/o cable	JA9114029-01
TB-68CI	68-Pin SCSI Shielded I/O Connector Block with current converter	JY2010068-02
TB-68CI-16	68-Pin SCSI Shielded I/O Connector Block with 16ch current converter	JY2010068-03

规格

Analog Input Specifications			
Analog Input	PXIe/PCIe-5510	PXIe/PCIe-5511	PXIe/PCIe-5512
Number of channels	32 SE/16 Diff		
ADC resolution(Bits)	18		
Single Channel Sampling Rate	2MHz	1.25MHz	500KHz
Multichannel Average Sampling Rate	1MHz	625KHz	250KHz
Clock	100MHz		
Input range(V)	±10/±5/±2/±1/±0.5/±0.2/±0.1		
Input mode	RSE / NRSE / Differential		
Input impedance	SE: 8pF；High Resistance Diff: 15pF		
Coupling method	DC		
Overvoltage protection	±25V		
CMRR	85dB		
Crosstalk	Adjacent Ch:-80dB, Non-adjacent:-95DB;Differential:-65DB		
DNL	<1LSB		
INL	70ppm of Range Typical		
Operating Temperature	0º ～ 50Cº		
Input FIFO	64M Samples		
Trigger source	Digital, Analog, Software Optional		
Trigger mode	Rising/Fall Edge, Range Trigger		
Analog trigger voltage range	-10V/10V Software Programmable		
Overvoltage Protection	Continuous 20mA -25V ～ 25V；Instantaneous 40mA -25 ～ 25V；		

Analog Output Specifications	
Analog Output	PXIe/PCIe-5510/5511/5512
Number of channels	4
DAC resolution	16 bits
Sampling rate(Hz)	1 Ch: 2.86M; 2Ch 2M; 3 Ch: 1.54M; 4 Ch: 1.25M
Clock	100MHz
Clock accuracy	Jitter <20ps
Output range(V)	±10/±5
Output mode	RSE
Output impedance	10 Ohm
Coupling method	DC
Output FIFO	32M Samples
Trigger source	Digital, Software Optional
Trigger mode	Rising/Fall Edge

Digital IO Specifications	
DIO	PXIe/PCIe-5510/5511/5512
Number of channels	Port（0,1,2,3）
Ground reference	D GND
Directionalcontrol	Independent control of each port
Clock	10MHz
DI FIFO	16MS
DO FIFO	16MS
Initial state	Input
Digital Input	Logic Low VIL=0:1.0V; Logic High VIH =(2V ～ 5.3V)
Digital Output	Logic Low VOL/IOL 0V/24mA; Logic HighVOH/IOH (2.6V ～ – 5V)/(-24mA ～ – 0mA)
Overvoltage Protection	Continuous 30mA -3.9V ～ 8.9V; Instantaneous 200mA -25 ～ 25V; Instantaneous current pulse width duty cycle does not exceed 15%

Counter/Timer Specifications	
CI/CO	PXIe/PCIe-5510/5511/5512
Number of channels	4
Resolution	32
CI	edge count,period measurement,frequency measurement, pulse width measurement,two-edge interval measurement, orthogonal coding, etc.
CO	Single,finite and continuous pulse
Clock	200MHz
FIFO	4M Samples
Input	Gate，Source，Aux，SampleClock
Output	OUT